EE 2381 DIGITAL LOGIC

Course Syllabus

Professor Clark Kinnaird

Course Description:
Digital computers and information; combinational logic circuits; combinational logic design; sequential circuits including finite-state machines; registers and counters; memory and programmed logic design. Design and simulation of digital computer logic circuits are studied. Concurrent registration in EE 2181 required.

Concurrent Registration:	EE 2181 *EE Lab: Digital Computer Logic*
Textbook:	*Digital Design*, Mano & Ciletti, Fourth Edition
Lectures:	TuTh 8:00 - 9:20 AM Junkins Building 203
Office Hours:	To be arranged, & by Appointment
Office Location:	Caruth Hall 379

Email kinnaird@smu.edu Web: http://www.engr.smu.edu/~kinnaird

Grading Policy:

In Class Exams - 2	50 %
Final Exam	30 %
Homework	20 %

Class Policies:

Attendance: I do not grade based on daily attendance. I may drop a student administratively for non-attendance combined with failure to submit graded materials.

Make-Ups: Please let me know in advance if you are unable to submit graded materials by the scheduled due date so an alternative due date can be arranged. I do reserve the right to administer a different, but comparable, make-up examination.

Late Homework: Students should submit homework by the scheduled due date. I will accept late homework (with a late penalty) up to the time homework solutions are distributed.

Class Disruption: Please mute your electronics during class.

Lateness: Please enter and quietly take a seat so as not to wake the class.

Disability Accommodations:
If you need academic accommodations for a disability, you must first contact Ms. Rebecca Marin, Coordinator of Services for Students with Disabilities (214-768-4557) to verify the disability and to establish eligibility for accommodations. Then you should schedule an appointment with me so that appropriate arrangements can be made. (Refer to University Policy No. 2.4.)

Religious Observance:
Religiously observant students wishing to be absent on holidays that require missing class should notify me in writing at the beginning of the semester, and should discuss with me, in advance, acceptable ways of making up any work missed because of the absence. (Refer to University Policy No. 1.9.)

Excused Absences for University Extracurricular Activities:
Students participating in an officially sanctioned, scheduled University extracurricular activity will be given the opportunity to make up class assignments or other graded assignments missed as a result of their participation. It is the responsibility of the student to make arrangements with me prior to any missed scheduled examination or other missed assignment for making up the work. (Refer to University Undergraduate Catalogue)

Incomplete Policy:
An Incomplete (I) may be given if the majority of the course requirements have been completed with passing grades but for some justifiable reason, acceptable to the instructor, the student has been unable to complete the full requirements of the course. Before an (I) is given, the instructor should stipulate, in writing, to the student the requirements and completion date that are to be met and the grade that will be given if the requirements are not met by the completion date. The maximum period of time allowed to clear the Incomplete grade is 12 months (except for graduate thesis and dissertation courses). If the Incomplete grade is not cleared by the date set by the
instructor or by the end of the 12-month deadline, the (I) may be changed to an F or to another grade specified by the instructor. The grade of (I) is not given in lieu of an F, WP, or other grade, each of which is prescribed for other specific circumstances. If the student's work is incomplete and the quality has not been passing, an F will be given. The grade of (I) does not authorize the student to attend the course during a later semester. Graduation candidates must clear all Incompletes prior to the deadline in the official University Calendar, which may allow less time than 12 months. Failure to do so can result in removal from the degree candidacy list and/or conversion of the (I) to the grade indicated by the instructor at the time the (I) was given.

Academic Honesty:
Academic dishonesty may be defined broadly as a student' misrepresentation of his or her academic work or of the circumstances under which the work is done. This includes plagiarism in all papers, projects, take-home exams, or any other assignments in which the student represents work as being his or her own. It also includes cheating on examinations, unauthorized access to test materials, and aiding another student to cheat or participate in an act of academic dishonesty. Failure to prevent cheating by another may be considered as participation in the dishonest act.

The Honor Code of Southern Methodist University:
The Honor Code is posted at www.smu.edu/studentlife/PCL_05_HC.asp and states:

“Intellectual integrity and academic honesty are fundamental to the processes of learning and of evaluating academic performance, and maintaining them is the responsibility of all members of an educational institution. The inculcation of personal standards of honesty and integrity is a goal of education in all the disciplines of the University.

“The faculty has the responsibility of encouraging and maintaining an atmosphere of academic honesty by being certain that students are aware of the value of it, that they understand the regulations defining it, and that they know the penalties for departing from it. The faculty should, as far as is reasonably possible, assist students in avoiding the temptation to cheat. Faculty members must be aware that permitting dishonesty is not open to personal choice. A professor or instructor who is unwilling to act upon offenses is an accessory with the student offender in deteriorating the integrity of the University.

“Students must share the responsibility for creating and maintaining an atmosphere of honesty and integrity. Students should be aware that personal experience in completing assigned work is essential to learning. Permitting others to prepare their work, using published or unpublished summaries as a substitute for studying required materials, or giving or receiving unauthorized assistance in the preparation of work to be submitted are directly contrary to the honest process of learning. Students who are aware that others in a

course are cheating or otherwise acting dishonestly have the responsibility to inform the professor and/or bring an accusation to the Honor Council.

“Students and faculty members must mutually share the knowledge that any dishonest practices permitted will make it more difficult for the honest students to be evaluated and graded fairly and will damage the integrity of the whole University. Students should recognize that both their own interest, and their integrity as individuals, suffer if they condone dishonesty in others.”

The Honor System:
The *SMU Undergraduate Catalog* states:

“All students at SMU, with the exception of those enrolled in School of Law, Perkins School of Theology, and Cox M.B.A. School, are subject to the jurisdiction of the Honor Code and as such will be required to sign a pledge to uphold the Honor Code (www.smu.edu/studentlife). The Honor Council is composed of approximately 27 students selected through an application and interview process by the Honor Council Executive Board and five faculty members nominated by the Faculty Senate. The council's responsibility is to maintain and promote academic honesty.

“Academic dishonesty is defined broadly as a student's misrepresentation of his or her academic work or of the circumstances under which that work is done. This includes plagiarism in all papers, projects, take-home exams, or any other assignments in which the student submits another's work as being his or her own. It also includes cheating on examinations, unauthorized access to test materials, and/or assisting another student in gaining any unfair academic advantage. Lastly, it includes academic sabotage, defined as intentionally taking any action that negatively affects the academic work of another student. Failure to prevent or report academic dishonesty by another may be considered participation in a dishonest act.

“Suspected cases of academic dishonesty may be handled administratively by the appropriate faculty member in whose class the alleged infraction occurred or referred to the Honor Council for resolution. Suspected violations reported to the Honor Council by a student or by an instructor will be investigated and, if the evidence warrants, a hearing will be held by a Board composed of at least five members of the Honor Council.

“Any appeal of an action taken by the Honor Council shall be submitted to the University Judicial Council in writing no later than four calendar days (excluding school holidays) after notification of the Honor Council's decision.”

Course Calendar & Topics: *(subject to change as required)*

Lecture	Topic	Title
1	1	Introduction and Overview
	2	I Digital Computers and Information
2	3	I.A Base Conversions
	4	I.B Base *R* Arithmetic
3	5	I.C Binary Codes
	6	II Combinational Logic Circuits
4	7	II.A Boolean Algebra
5	8	II.B Boolean Function Representations
	9	II.C Karnaugh Maps
6	10	II.D Minimal Realizations
7	11	II.E Alternate Realizations
8	12	II.F Delays
	13	II.G Timing Diagrams
9	14	III Combinational Logic Design
	15	III.A Verilog Logic Simulation
10	16	III.B Decoders/Demultiplexers
11	17	III.C Data Selectors/Multiplexers
12	**Exam I**	
13	18	III.D Binary Arithmetic – Addition
14	19	III.E Binary Arithmetic – Subtraction
15	20	III.F Binary Arithmetic – Formal
16	21	IV.A Sequential Circuits
17	22	IV.B Edge-Triggered Flip-Flops
18	23	IV.C Design of Counters (D Flip-Flops)
	24	IV.D Design of Counters (J-K Flip-Flops)
19	25	IV.E Timing Diagrams with Flip-Flops
20	26	IV.F Finite-State Machines (Moore)
21	**Exam II**	
22	27	IV.G Finite-State Machines (Mealy)
	28	IV.H Finite-State Machine Design (Example 1)
	29	IV.I Finite-State Machine Design (Example 2)
23	30	IV.J State Table Reduction
24	31	IV.K Finite-State Machine Design (Example 2 Revisited)
25	32	IV.L Finite-State Machine Design (Verilog Representations).
26	33	V Registers and Counters
27	34	VI.A Memory & Programmable Logic Design (RAM and ROM)
28	35	VI.B Memory & Programmable Logic Design (PLA and PAL)
29	36	VII Course Wrap-up
Final Exam		